Re

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,990	03/29/2001	Isao Minematsu	57454-060	3710

7590 11/17/2006

McDERMOTT, WILL & EMERY
600 13th Street, N. W.
Washington, DC 20005-3096

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,990	MINEMATSU, ISAO	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-10 are presented for examination. Claims 1-14 have been canceled.

In view of the supplemental appeal brief filed on 08/25/06 , PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim s 1-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant's specification, page 12, lines 3-12, fig.9A, taught a single instruction code POP instruction with two operational codes (pop(1) with no register and pop(2) with a register as shown in fig.9A). However, claim 1 is directed to the data transfers in correspondence to single instruction code having a single operation code (see claim 1, lines 7-9). No single instruction code having a single operation code can be found in the specification. Furthermore, even if the pop(2) (see fig.9A) is considered as the single instruction code having single operation code, it only has the data transfer between registers, not the data transfer between the registers and the memory as claimed. The data transfer from the stack to the working register (Tr0) is a data transfer between a register and a memory. No description of the data transfer between registers and memory corresponding to the single instruction code having single operating code can be found in the specification. Therefore, it raised a doubt as whether applicant had possession of the clamed subject matter at the time of the filing.

3. Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant's specification, page 12, lines 3-12, fig.9A, taught a single instruction code POP instruction with two operational codes (pop(1) with no register and pop(2) with a register as shown in fig.9A). However, claim 1 is directed to the data

transfers in correspondence to single instruction code having a single operation code (see claim 1, lines 7-9). No single instruction code having a single operation code for the data transfer between the registers and data transfer between the registers and the memory is being taught in the specification. The POP instruction is a single instruction code having two pop operation codes, one with no register (pop(1)) and another with a register(pop (2) (see efig.9A). Furthermore, even if the pop(2) (see fig.9A) is considered as the single instruction code having single operation code, it only has the data transfer between registers, not data transfer between the registers and the memory. The data transfer from the stack to the working register (Tr0) is a data transfer between a register and a memory, not between registers and a memory as claimed. No teaching of how the data transfer is implemented between registers and memory corresponding to the single instruction code having single operation code can be found in the specification Therefore, the enablement is not satisfactorily resolved , and consequently raised a doubt as to the enablement (see 858 F.2d 731, 737 8 USPQ2d 1400, 1404 (Fed. Cir. 1998), see also MPEP 21654.01, 2164.04).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Col et al. (6,349,383) in view of Volentine et al. (6,363,473).

As to claim 1, the ground of rejection is based on the transfer between the registers and memory.

5. Col taught at least :

a) a program control unit controlling fetch of an instruction code (see fetch stage , not explicitly shown in fig.4, but see fetch stage for fetching the macroinstruction in col.12, lines 27-35) ;

b) an instruction decode unit (see fig.4 translator 420 for decoding a macro instruction in col.12, lines 63-66) decoding the fetched instruction code;

c) an address operation unit (see address registers 442,444, 446 in fig.4) operating an address of a memory on the basis of the result of decoding by the instruction decode unit (see col.12, lines 27-50); and

d) a data operation unit (see fig.4 442,444,446, 422, 448) operating data on the basis of the result of decoding by the instruction decode unit, wherein data operation unit executed data transfer between the registers and the memory in correspondence to single instruction code [POP2 AX, BX] having a single operation code [POP2] fetched by program control unit (see the pop of data into register AX and BX in col.15, lines 17-46). Col is directed to a single instruction code [POP2 AX, BX] having a single operation code [POP2], not double codes.

6. Col did not specifically show the data transfer between registers as claimed. However, Volentine disclosed a system including a single instruction code [SPUSH MACRO REG1] (see col.11, lines 10-25) having a single operation code [SPUSH] for transferring between registers (see the move of content of REG1 to bp register in col.11, line 15, see also 8 [314]). It would have been obvious to one of ordinary skill in the art to use Volentine in Col for including the data transfer between registers as claimed because the use of Volentine could provide Col the capability to generate more than one operations in a single predefined instruction code, therefore, reducing the overall latency of the complex instructions, and it could be achieved by predefining the Volentine's single instruction for transfer between the registers into the configuration file of Col with modified system parameters (e.g. the instruction type, code length) so that the specific transfer instruction of Volentine could be recognized by Col, and because Col also taught that the future improvement was to include a microinstruction which directed the microprocessor to access a single cache line during a single instruction cycle to access multiple prescribed data entities (see col.21, lines 40-46), which was a suggestion of the need for the data transfer between multiple data entities, such as transfer between registers in a single instruction, in doing so, provided a motivation.

7. As to claim 2, Col also taught a single push (see push EAX in col.16, lines 15-24).

8. As to claim 3, Volentine also increased the pointer (see step 344 in fig,4).

9. As to claims 4,8, Col 's first register was a work register (see fig.6 [EAX]). See also Volentine's register REG1 in fig.8 [REG1].

10. As to claims 5,9, see the control register bp in 314 in fiog.8.

11. As to claim 6, Col also included single pop (see pop in col.14, lines 40-50).

12. As to claim 7, see Volentine's fig.8 [increment pointer 344].

13. As to clam 10, see the saved new pointer index in the push in fig.8 [346].

14. Claim 1 is also rejected under alternative interpretation that the data transfer is between one of the registers and memory.

15. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mandavilli (6,546,480) in view of Morrison et al. (5,918,031) .

16. As to claim 1, Mandavilli taught a system including at least a single instruction code MCMV for data transfer between registers (see copy of Rm register to Rd register in col.24, lines 5-11) . Mandavilli did not specifically show the data transfer between the register and memory as clamed. However, Morrison taught a system in which a common sequence of instructions were collapsed into a single code (seeco!.5,

lines 22-37, col.8, lines 30-35) including at least a data transfer between the register and memory (see MOV reg , mem in col.7, line 35). It would have been obvious to one of ordinary skill in the art to use Morrison in Mandavilli for including the data transfer between the register and memory because the use of Morrison could provide the ability of Mandavilli to integrated multiple operations between the transfer operations of registers and memory in an predetermined format, thereby minimizing the hardware overheads of the system, and because Mandavilli also taught data temporally latched for the next stage of processing (see col.5, lines 61-67, col.6, lines 1-3, see also the SIMD and multimedia processing in col.4, lines 5-6, col.5, lines 24-37), which was an indication of the need for saving data in a memory for the purpose of subsequent pipeline stage processing , and for the above reasons , provided a motivation.

17. As to the instruction fetch and the instruction decode, since no specific type of fetch and decoder has been reflected into the claim, examiner holds that instruction fetch and instruction decode in general were already known in the art.

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Koppala et al. (6,108,768) is cited for the teaching of the transferring or pushing data from a memory or a register into a stack (see col.8, lines 22-36).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP

EDDIE CHAN
SUPERVISORY PATENT EXAM
TECHNOLOGY CENTER 21